New Generation of WICOP

High-Power LED – WICOP Z8 Y19

SZ8-Y19-XX-XX (Cool, Neutral, Warm)

LM-80

Product Brief

Description

- The WICOP series is designed for high flux output applications with high current operation capability.
- Compact footprint(1.81x1.81mm) enables system level cost saving
- It incorporates state of the art SMD design and low thermal resistant material.

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- The WICOP is ideal light sources for directional lighting applications such as Spot Lights, various outdoor applications, automotive lightings and high performance torches .

Features and Benefits

- Designed for high current operation
- Low Thermal Resistance
- A wide CCT range of 2,600~7,000K
- ANSI compliant Binning
- RoHS compliant
- Phosphor film directly attached to chip surface

Key Applications

- Residential - Replacement lamps
- Commercial/Industrial – Retail Display
- Outdoor area - Flood/Street light, High Bay

Table 1. Product Selection Table

Part Number	CCT			CRI
	Color	Min.	Max.	Min
SZ8-Y19-W0-C7	Cool White	4,700K	7,000K	70
SZ8-Y19-W0-C8	Cool White	4,700K	7,000K	80
SZ8-Y19-W0-C9	Cool White	4,700K	7,000K	90
SZ8-Y19-WN-C7	Neutral White	3,700K	4,700K	70
SZ8-Y19-WN-C8	Neutral White	3,700K	4,700K	80
SZ8-Y19-WN-C9	Neutral White	3,700K	4,700K	90
SZ8-Y19-WW-C7	Warm White	2,600K	3,700K	70
SZ8-Y19-WW-C8	Warm White	2,600K	3,700K	80
SZ8-Y19-WW-C9	Warm White	2,600K	3,700K	90

Table of Contents

Performance Characteristics

Table 2. Electro Optical Characteristics, T_j=85℃ (CRI 70)

Part Number	CCT [K] [1]		Min. Luminous Flux [2] Φ_V [3] [lm] Tj=85 °C					CRI [4], R_a
	Min.	Max.	Group	350mA	700mA	1.0A	1.5A	Min.
SZ8-Y19-W0-C7	4700	7000	W5	167	299	394	535	70
			W4	160	285	376	510	
			W3	152	271	357	485	
			W2	142	254	335	455	
SZ8-Y19-WN-C7	3700	4700	W5	167	299	394	535	70
			W4	160	285	376	510	
			W3	152	271	357	485	
			W2	142	254	335	455	
SZ8-Y19-WW-C7	2600	3700	W3	152	271	357	485	70
			W2	142	254	335	455	
			W1	133	237	313	424	
			V3	125	223	294	399	

Notes :

(1) Correlated Color Temperature is derived from the CIE 1931 Chromaticity diagram.

Color coordinate : ±0.005, CCT ±5% tolerance.

(2) Seoul Semiconductor maintains a tolerance of ±7% on flux and power measurements.

(3) Φ_V is the total luminous flux output as measured with an integrating sphere.

(4) Tolerance is ±2.0 on CRI measurements.

Performance Characteristics

Table 2. Electro Optical Characteristics, T_j=85℃ (CRI 80)

Part Number	CCT [K] [1]		Min. Luminous Flux [2] Φ_V [3] [lm] Tj=85 °C					CRI [4], R_a
	Min.	Max.	Group	350mA	700mA	1.0A	1.5A	Min.
SZ8-Y19-W0-C8	4700	7000	W3	152	271	357	485	80
			W2	142	254	335	455	
			W1	133	237	313	424	
			V3	125	223	294	399	
SZ8-Y19-WN-C8	3700	4700	W3	152	271	357	485	80
			W2	142	254	335	455	
			W1	133	237	313	424	
			V3	125	223	294	399	
SZ8-Y19-WW-C8	2600	3700	W1	133	237	313	424	80
			V3	125	223	294	399	
			V2	116	208	274	372	
			V1	109	195	257	349	

Notes :

(1) Correlated Color Temperature is derived from the CIE 1931 Chromaticity diagram.

Color coordinate : ±0.005, CCT ±5% tolerance.

(2) Seoul Semiconductor maintains a tolerance of ±7% on flux and power measurements.

(3) Φ_V is the total luminous flux output as measured with an integrating sphere.

(4) Tolerance is ±2.0 on CRI measurements.

Performance Characteristics

Table 2. Electro Optical Characteristics, T_j=85℃ (CRI 90)

Part Number	CCT [K] [1]		Min. Luminous Flux [2] Φ_V [3] [lm] Tj=85 °C					CRI [4], R_a
	Min.	Max.	Group	350mA	700mA	1.0A	1.5A	Min.
SZ8-Y19-W0-C9	4700	7000	W1	133	237	313	424	90
			V3	125	223	294	399	
			V2	116	208	274	372	
			V1	109	195	257	349	
SZ8-Y19-WN-C9	3700	4700	W1	133	237	313	424	90
			V3	125	223	294	399	
			V2	116	208	274	372	
			V1	109	195	257	349	
SZ8-Y19-WW-C9	2600	3700	V2	116	208	274	372	90
			V1	109	195	257	349	
			U3	102	182	240	326	
			U2	96	172	227	308	

Notes :

(1) Correlated Color Temperature is derived from the CIE 1931 Chromaticity diagram.

Color coordinate : ±0.005, CCT ±5% tolerance.

(2) Seoul Semiconductor maintains a tolerance of ±7% on flux and power measurements.

(3) Φ_V is the total luminous flux output as measured with an integrating sphere.

(4) Tolerance is ±2.0 on CRI measurements.

Performance Characteristics

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Forward Current [1]	I_F	-	-	1.5 [4] 2.0 [3]	A
Power Dissipation	P_D	-	-	7.8	W
Junction Temperature	T_j	-	-	145	ºC
Operating Temperature	T_{opr}	- 40	-	125	ºC
Storage Temperature	T_{stg}	- 40	-	125	ºC
Viewing angle	θ		140		degree
Forward voltage (350mA, 85℃)	V_F		2.71		V
Forward voltage (700mA, 85℃)	V_F		2.86		V
Thermal resistance (J to S) [2]	$R\theta_{J-S}$	-	3 [3] 4.5 [4]	-	K/W
ESD Sensitivity(HBM)			Class 2 JESD22-A114-E		

Notes :

(1) At Junction Temperature 85℃ condition.

(2) $R\theta_{J-S}$ is tested at 700mA.

(3) Using Metal PCB (Dielectric layer 5W/m·K and Cu pattern of 2oz).

(4) Using Metal PCB (Normal type).

- Thermal resistance can be increased substantially depending on the heat sink design/operating condition, and the maximum possible driving current will decrease accordingly.

Characteristics Graph

Fig 1. Color Spectrum

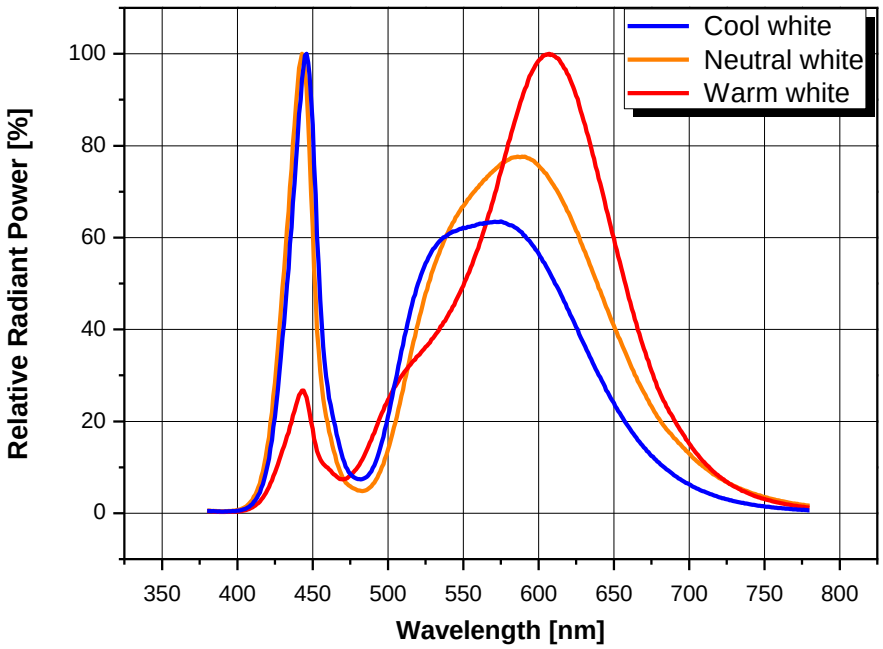
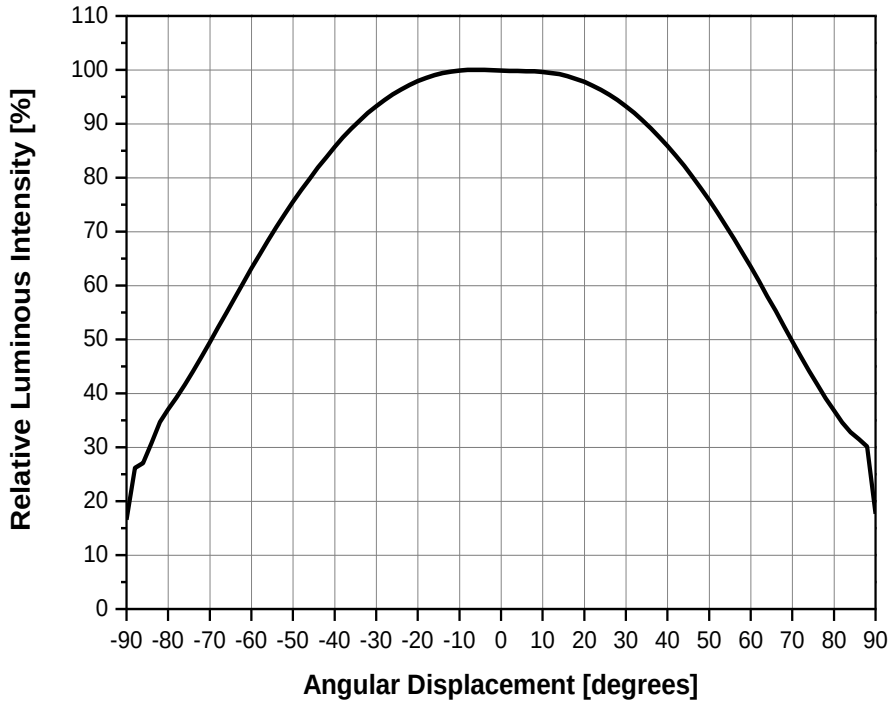


Fig 2. Typical Spatial Distribution



Characteristics Graph

Fig 3. Forward Voltage vs. Forward Current, T_j=85℃

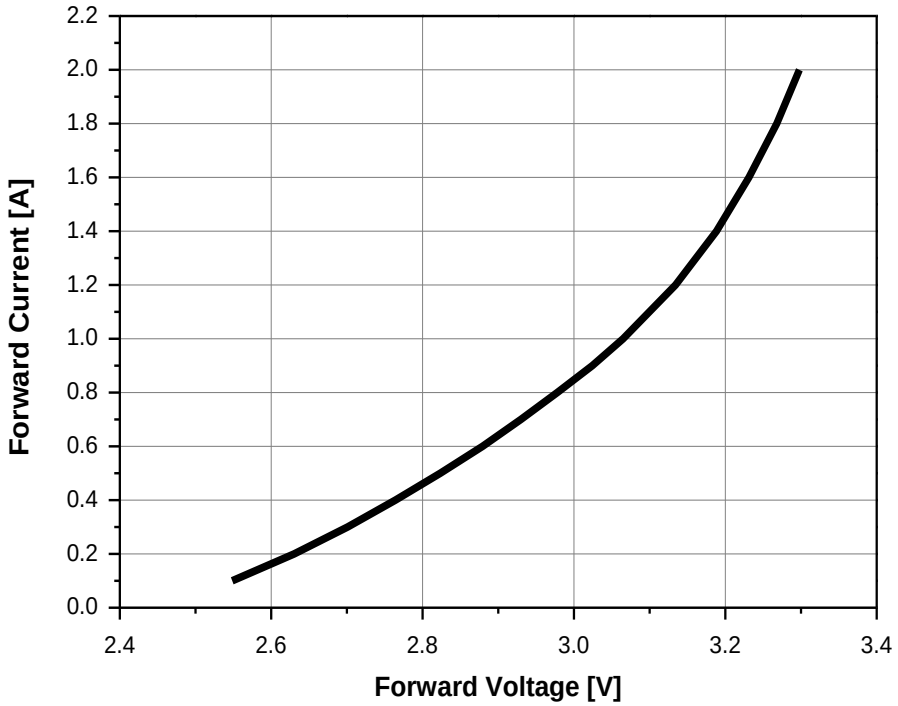
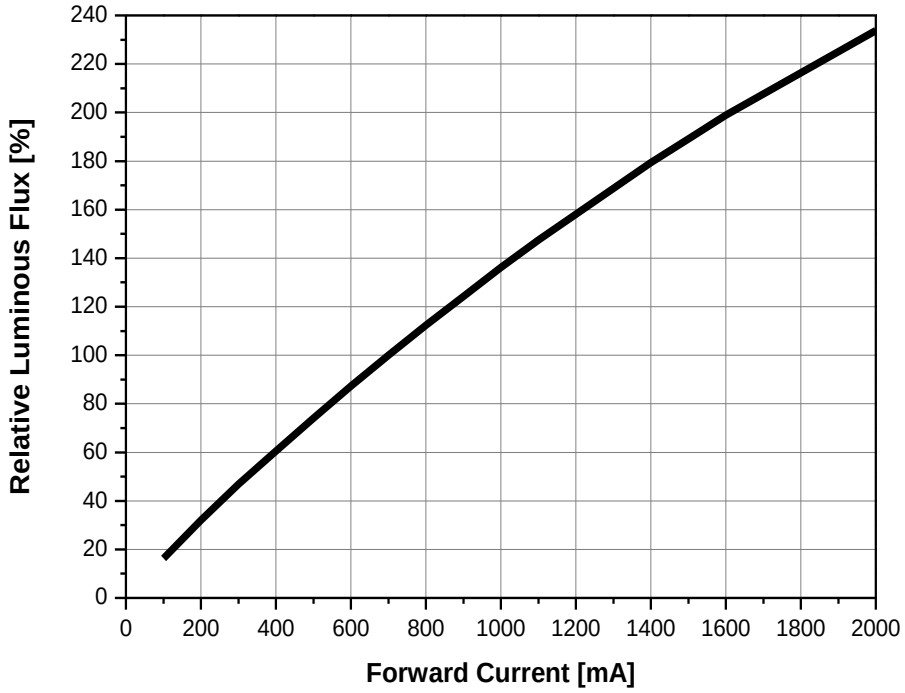


Fig 4. Forward Current vs. Relative Luminous Flux, T_j=85℃



Characteristics Graph

Fig 5. Forward Current vs. CIE X, Y Shift, T_j=85℃

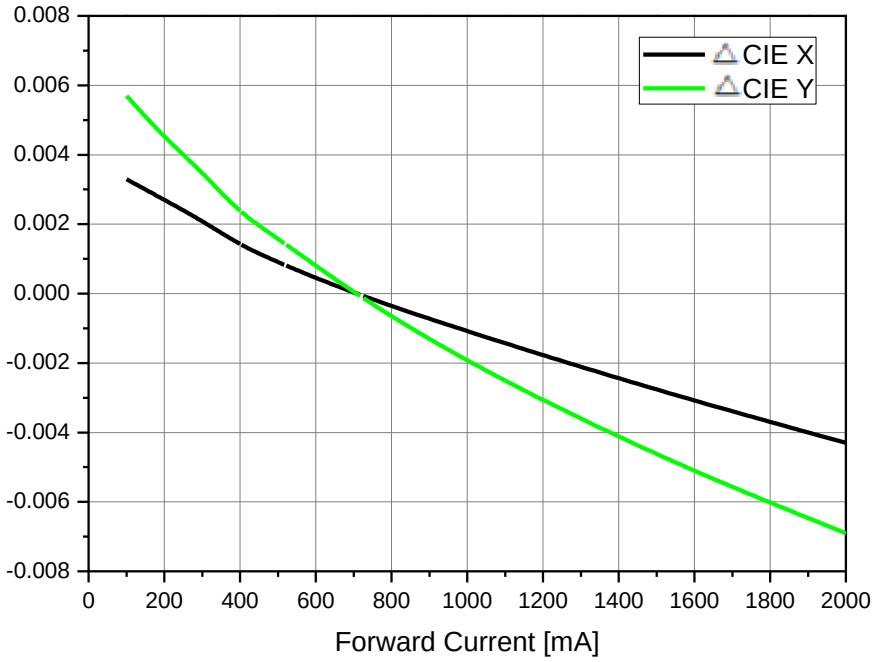
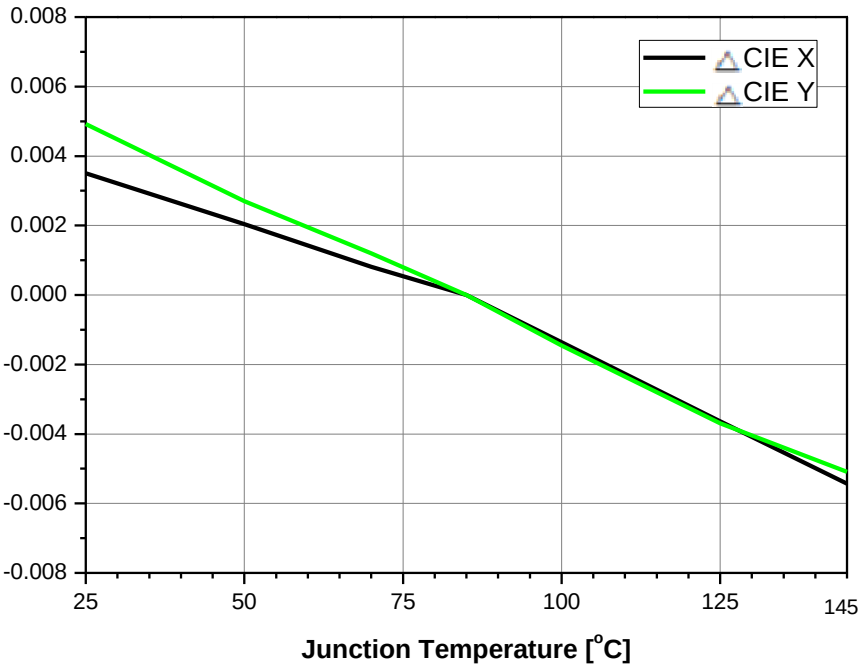


Fig 6. Junction Temp. vs. CIE X, Y Shift, I_F=700mA



Characteristics Graph

Fig 7. Relative Light Output vs. Junction Temperature, I_F=700mA

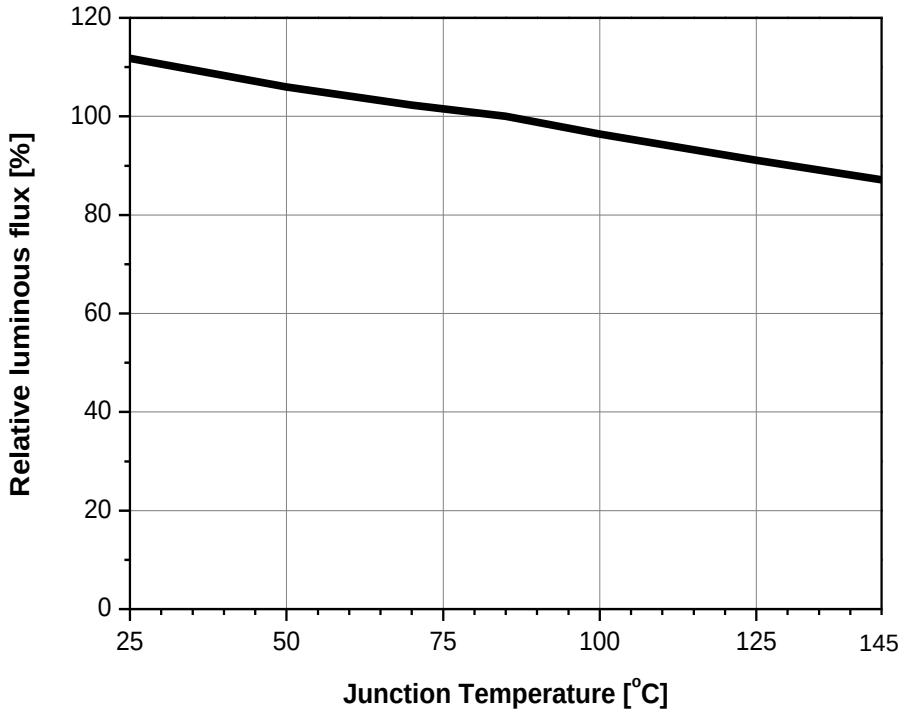
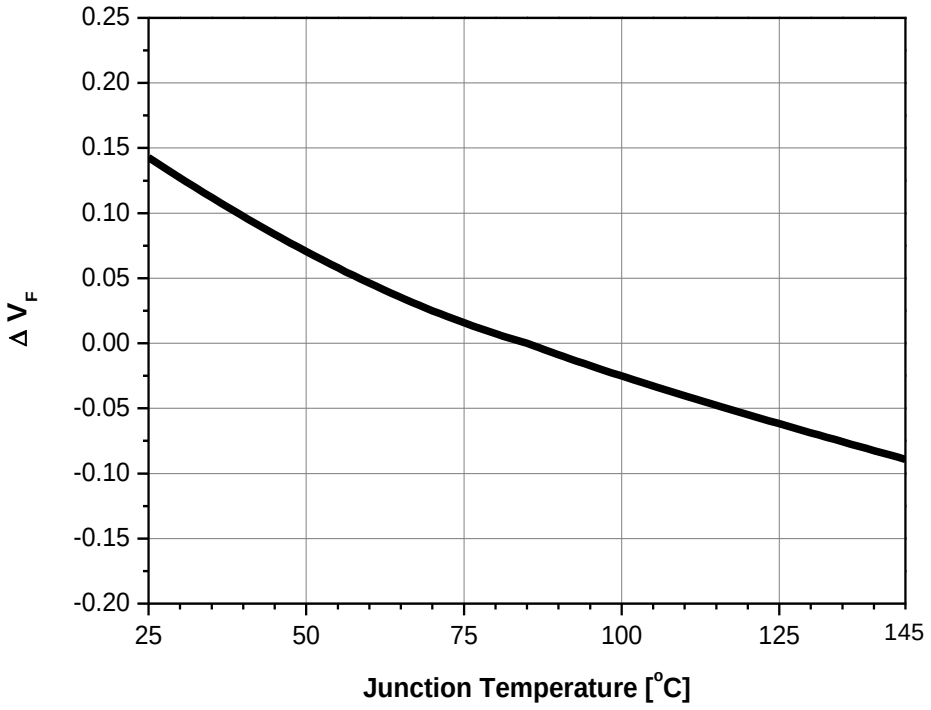
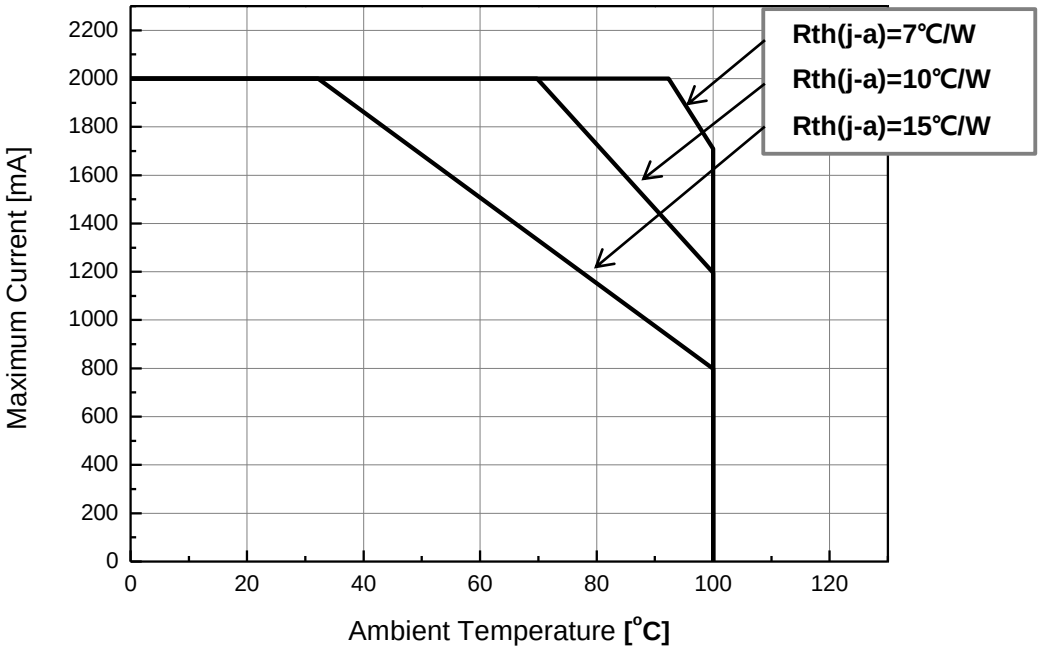


Fig 8. Relative Forward Voltage vs. Junction Temperature, I_F=700mA



Characteristics Graph

Fig 9. Maximum Forward Current vs. Ambient Temperature, T_j(max.)=145℃, I_F=2A



Color Bin Structure

Table 4. Bin Code description, I_F=700mA, T_j=85℃ (CRI 70)

Part Number	Luminous Flux [lm]			Color Chromaticity Coordinate	Typical Forward Voltage [V_F] [1] *		
	Bin Code	Min.	Max.		Bin Code	Min.	Max.
SZ8-Y19-W0-C7	W2	254	271	Refer to page. 15	G	2.75	3.00
	W3	271	285				
	W4	285	299		H	3.00	3.25
	W5	299	313				
SZ8-Y19-WN-C7	W2	254	271	Refer to page. 16~17	G	2.75	3.00
	W3	271	285				
	W4	285	299		H	3.00	3.25
	W5	299	313				
SZ8-Y19-WW-C7	V3	223	237	Refer to page. 18~20	G	2.75	3.00
	W1	237	254				
	W2	254	271		H	3.00	3.25
	W3	271	285				

Table 5. Luminous Flux rank distribution (CRI 70) ■ **Available Rank**

CCT	CIE	Luminous Flux Rank						
6,000 ~ 7,000K	A	V2	V3	W1	W2	W3	W4	W5
5,300 – 6,000K	B	V2	V3	W1	W2	W3	W4	W5
4,700 ~ 5,300K	C	V2	V3	W1	W2	W3	W4	W5
4,200 ~ 4,700K	D	V2	V3	W1	W2	W3	W4	W5
3,700 ~ 4,200K	E	V2	V3	W1	W2	W3	W4	W5
3,200 ~ 3,700K	F	V2	V3	W1	W2	W3	W4	W5
2,900 ~ 3,200K	G	V2	V3	W1	W2	W3	W4	W5
2,600 ~ 2,900K	H	V2	V3	W1	W2	W3	W4	W5

Notes :

(1) Tolerance is ±0.06V on forward voltage measurements.

(2) All measurements were made under the standardized environment of Seoul Semiconductor
In order to ensure availability, single color rank will not be orderable.

Color Bin Structure

Table 4. Bin Code description, I_F=700mA, T_j=85℃ (CRI 80)

Part Number	Luminous Flux [lm]			Color Chromaticity Coordinate	Typical Forward Voltage [V_F] [1] *		
	Bin Code	Min.	Max.		Bin Code	Min.	Max.
SZ8-Y19-W0-C8	V3	223	237	Refer to page. 15	G	2.75	3.00
	W1	237	254				
	W2	254	271		H	3.00	3.25
	W3	271	285				
SZ8-Y19-WN-C8	V3	223	237	Refer to page. 16~17	G	2.75	3.00
	W1	237	254				
	W2	254	271		H	3.00	3.25
	W3	271	285				
SZ8-Y19-WW-C8	V1	195	208	Refer to page. 18~20	G	2.75	3.00
	V2	208	223				
	V3	223	237		H	3.00	3.25
	W1	237	254				

Table 5. Luminous Flux rank distribution (CRI 80)

Available Rank

CCT	CIE	Luminous Flux Rank					
6,000 ~ 7,000K	A	V1	V2	V3	W1	W2	W3
5,300 – 6,000K	B	V1	V2	V3	W1	W2	W3
4,700 ~ 5,300K	C	V1	V2	V3	W1	W2	W3
4,200 ~ 4,700K	D	V1	V2	V3	W1	W2	W3
3,700 ~ 4,200K	E	V1	V2	V3	W1	W2	W3
3,200 ~ 3,700K	F	V1	V2	V3	W1	W2	W3
2,900 ~ 3,200K	G	V1	V2	V3	W1	W2	W3
2,600 ~ 2,900K	H	V1	V2	V3	W1	W2	W3

Notes :

(1) Tolerance is ±0.06V on forward voltage measurements.

(2) All measurements were made under the standardized environment of Seoul Semiconductor
In order to ensure availability, single color rank will not be orderable.

Color Bin Structure

Table 4. Bin Code description, I_F=700mA, T_j=85℃ (CRI 90)

Part Number	Luminous Flux [lm]			Color Chromaticity Coordinate	Typical Forward Voltage [V_F] [1] *		
	Bin Code	Min.	Max.		Bin Code	Min.	Max.
SZ8-Y19-W0-C9	V1	195	208	Refer to page. 15	G	2.75	3.00
	V2	208	223				
	V3	223	237		H	3.00	3.25
	W1	237	254				
SZ8-Y19-WN-C9	V1	195	208	Refer to page. 16~17	G	2.75	3.00
	V2	208	223				
	V3	223	237		H	3.00	3.25
	W1	237	254				
SZ8-Y19-WW-C9	U2	172	182	Refer to page. 18~20	G	2.75	3.00
	U3	182	195				
	V1	195	208		H	3.00	3.25
	V2	208	223				

Table 5. Luminous Flux rank distribution (CRI 90)

Available Rank

CCT	CIE	Luminous Flux Rank					
6,000 ~ 7,000K	A	U2	U3	V1	V2	V3	W1
5,300 – 6,000K	B	U2	U3	V1	V2	V3	W1
4,700 ~ 5,300K	C	U2	U3	V1	V2	V3	W1
4,200 ~ 4,700K	D	U2	U3	V1	V2	V3	W1
3,700 ~ 4,200K	E	U2	U3	V1	V2	V3	W1
3,200 ~ 3,700K	F	U2	U3	V1	V2	V3	W1
2,900 ~ 3,200K	G	U2	U3	V1	V2	V3	W1
2,600 ~ 2,900K	H	U2	U3	V1	V2	V3	W1

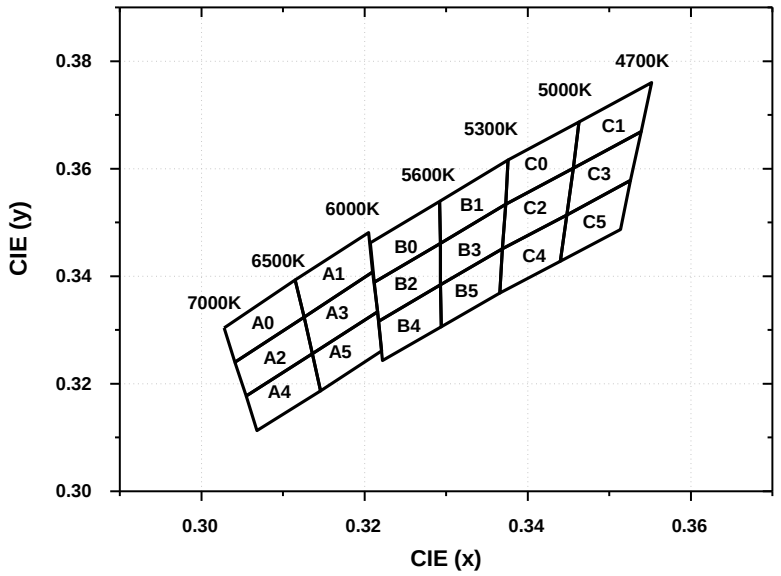
Notes :

(1) Tolerance is ±0.06V on forward voltage measurements.

(2) All measurements were made under the standardized environment of Seoul Semiconductor
In order to ensure availability, single color rank will not be orderable.

Color Bin Structure

CIE Chromaticity Diagram (Cool white), T_j=85℃, I_F=700mA



A0		A1		A2		A3	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3028	0.3304	0.3115	0.3393	0.3041	0.3240	0.3126	0.3324
0.3041	0.3240	0.3126	0.3324	0.3055	0.3177	0.3136	0.3256
0.3126	0.3324	0.3210	0.3408	0.3136	0.3256	0.3216	0.3334
0.3115	0.3393	0.3205	0.3481	0.3126	0.3324	0.3210	0.3408

A4		A5		B0		B1	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3055	0.3177	0.3136	0.3256	0.3207	0.3462	0.3292	0.3539
0.3068	0.3113	0.3146	0.3187	0.3212	0.3389	0.3293	0.3461
0.3146	0.3187	0.3221	0.3261	0.3293	0.3461	0.3373	0.3534
0.3136	0.3256	0.3216	0.3334	0.3292	0.3539	0.3376	0.3616

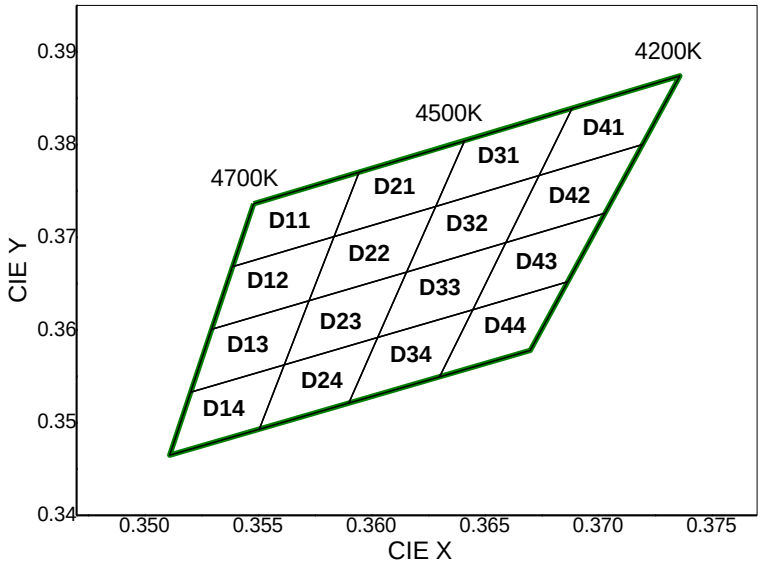
B2		B3		B4		B5	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3212	0.3389	0.3293	0.3461	0.3217	0.3316	0.3293	0.3384
0.3217	0.3316	0.3293	0.3384	0.3222	0.3243	0.3294	0.3306
0.3293	0.3384	0.3369	0.3451	0.3294	0.3306	0.3366	0.3369
0.3293	0.3461	0.3373	0.3534	0.3293	0.3384	0.3369	0.3451

C0		C1		C2		C3	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3376	0.3616	0.3463	0.3687	0.3373	0.3534	0.3456	0.3601
0.3373	0.3534	0.3456	0.3601	0.3369	0.3451	0.3448	0.3514
0.3456	0.3601	0.3539	0.3669	0.3448	0.3514	0.3526	0.3578
0.3463	0.3687	0.3552	0.3760	0.3456	0.3601	0.3539	0.3669

C4		C5	
CIE x	CIE y	CIE x	CIE y
0.3369	0.3451	0.3448	0.3514
0.3366	0.3369	0.3440	0.3428
0.3440	0.3428	0.3514	0.3487
0.3448	0.3514	0.3526	0.3578

Color Bin Structure

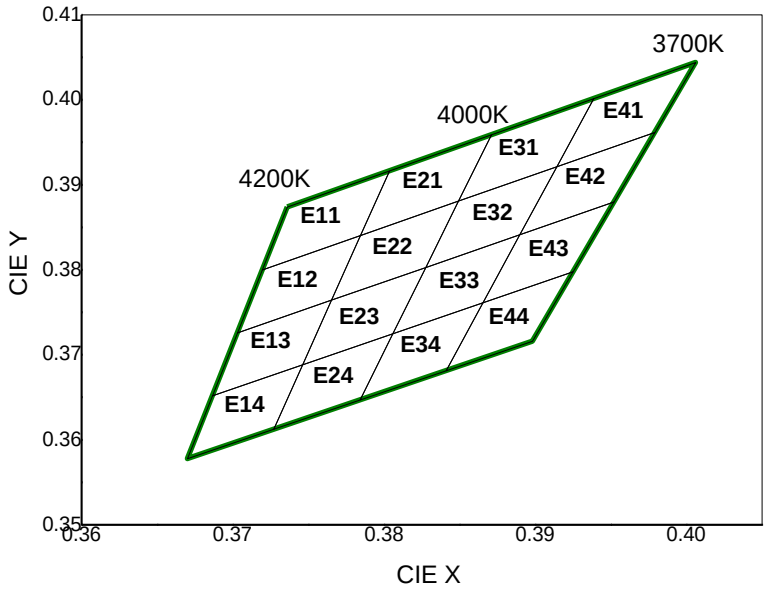
CIE Chromaticity Diagram (Neutral White), T_j=85℃, I_F=700mA



D11		D21		D31		D41	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3548	0.3736	0.3595	0.3770	0.3641	0.3804	0.3689	0.3839
0.3539	0.3668	0.3584	0.3701	0.3628	0.3733	0.3674	0.3767
0.3584	0.3701	0.3628	0.3733	0.3674	0.3767	0.3720	0.3800
0.3595	0.3770	0.3641	0.3804	0.3689	0.3839	0.3736	0.3874
D12		**D22**		**D32**		**D42**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3539	0.3668	0.3584	0.3701	0.3628	0.3733	0.3674	0.3767
0.3530	0.3601	0.3573	0.3632	0.3616	0.3663	0.3659	0.3694
0.3573	0.3632	0.3616	0.3663	0.3659	0.3694	0.3703	0.3726
0.3584	0.3701	0.3628	0.3733	0.3674	0.3767	0.3720	0.3800
D13		**D23**		**D33**		**D43**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3530	0.3601	0.3573	0.3632	0.3616	0.3663	0.3659	0.3694
0.3520	0.3533	0.3562	0.3562	0.3603	0.3592	0.3645	0.3622
0.3562	0.3562	0.3603	0.3592	0.3645	0.3622	0.3687	0.3652
0.3573	0.3632	0.3616	0.3663	0.3659	0.3694	0.3703	0.3726
D14		**D24**		**D34**		**D44**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3520	0.3533	0.3562	0.3562	0.3603	0.3592	0.3645	0.3622
0.3511	0.3465	0.3551	0.3493	0.3590	0.3521	0.3630	0.3550
0.3551	0.3493	0.3590	0.3521	0.3630	0.3550	0.3670	0.3578
0.3562	0.3562	0.3603	0.3592	0.3645	0.3622	0.3687	0.3652

Color Bin Structure

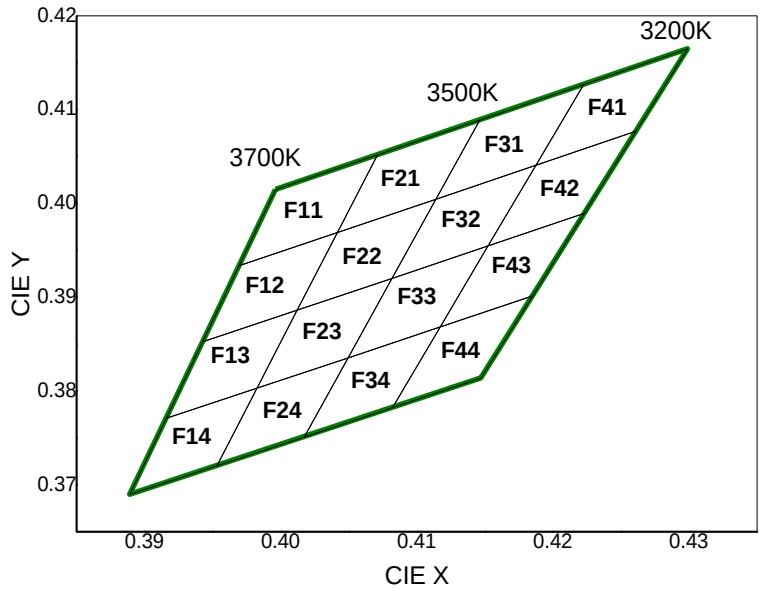
CIE Chromaticity Diagram (Neutral White), T_j=85℃, I_F=700mA



E11		E21		E31		E41	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3736	0.3874	0.3804	0.3917	0.3871	0.3959	0.3939	0.4002
0.3720	0.3800	0.3784	0.3841	0.3849	0.3881	0.3914	0.3922
0.3784	0.3841	0.3849	0.3881	0.3914	0.3922	0.3979	0.3962
0.3804	0.3917	0.3871	0.3959	0.3939	0.4002	0.4006	0.4044
E12		**E22**		**E32**		**E42**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3720	0.3800	0.3784	0.3841	0.3849	0.3881	0.3914	0.3922
0.3703	0.3726	0.3765	0.3765	0.3828	0.3803	0.3890	0.3842
0.3765	0.3765	0.3828	0.3803	0.3890	0.3842	0.3952	0.3880
0.3784	0.3841	0.3849	0.3881	0.3914	0.3922	0.3979	0.3962
E13		**E23**		**E33**		**E43**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3703	0.3726	0.3765	0.3765	0.3828	0.3803	0.3890	0.3842
0.3687	0.3652	0.3746	0.3689	0.3806	0.3725	0.3865	0.3762
0.3746	0.3689	0.3806	0.3725	0.3865	0.3762	0.3925	0.3798
0.3765	0.3765	0.3828	0.3803	0.3890	0.3842	0.3952	0.3880
E14		**E24**		**E34**		**E44**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3687	0.3652	0.3746	0.3689	0.3806	0.3725	0.3865	0.3762
0.3670	0.3578	0.3727	0.3613	0.3784	0.3647	0.3841	0.3682
0.3727	0.3613	0.3784	0.3647	0.3841	0.3682	0.3898	0.3716
0.3746	0.3689	0.3806	0.3725	0.3865	0.3762	0.3925	0.3798

Color Bin Structure

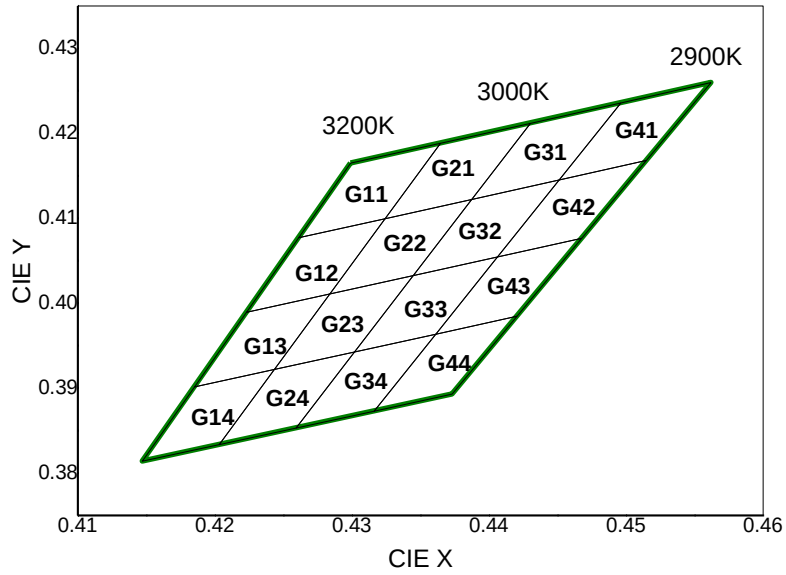
CIE Chromaticity Diagram (Warm White), T_j=85℃, I_F=700mA



F11		F21		F31		F41	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3996	0.4015	0.4071	0.4052	0.4146	0.4089	0.4223	0.4127
0.3969	0.3934	0.4042	0.3969	0.4114	0.4005	0.4187	0.4041
0.4042	0.3969	0.4114	0.4005	0.4187	0.4041	0.4261	0.4077
0.4071	0.4052	0.4146	0.4089	0.4223	0.4127	0.4299	0.4165
F12		**F22**		**F32**		**F42**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3969	0.3934	0.4042	0.3969	0.4114	0.4005	0.4187	0.4041
0.3943	0.3853	0.4012	0.3886	0.4082	0.3920	0.4152	0.3955
0.4012	0.3886	0.4082	0.3920	0.4152	0.3955	0.4223	0.3990
0.4042	0.3969	0.4114	0.4005	0.4187	0.4041	0.4261	0.4077
F13		**F23**		**F33**		**F43**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3943	0.3853	0.4012	0.3886	0.4082	0.3920	0.4152	0.3955
0.3916	0.3771	0.3983	0.3803	0.4049	0.3836	0.4117	0.3869
0.3983	0.3803	0.4049	0.3836	0.4117	0.3869	0.4185	0.3902
0.4012	0.3886	0.4082	0.3920	0.4152	0.3955	0.4223	0.3990
F14		**F24**		**F34**		**F44**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.3916	0.3771	0.3983	0.3803	0.4049	0.3836	0.4117	0.3869
0.3889	0.3690	0.3953	0.3721	0.4017	0.3751	0.4082	0.3783
0.3953	0.3721	0.4017	0.3751	0.4082	0.3783	0.4147	0.3814
0.3983	0.3803	0.4049	0.3836	0.4117	0.3869	0.4185	0.3902

Color Bin Structure

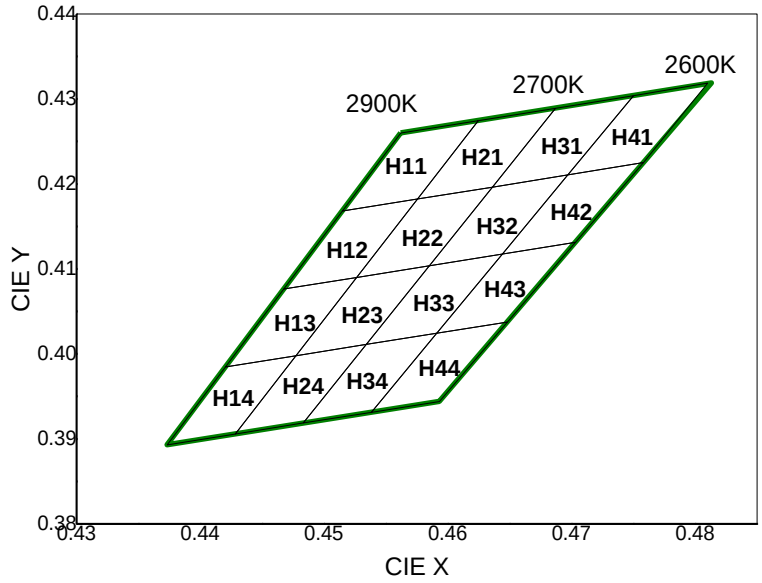
CIE Chromaticity Diagram (Warm White), T_j=85℃, I_F=700mA



G11		G21		G31		G41	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4299	0.4165	0.4364	0.4188	0.4430	0.4212	0.4496	0.4236
0.4261	0.4077	0.4324	0.4099	0.4387	0.4122	0.4451	0.4145
0.4324	0.4100	0.4387	0.4122	0.4451	0.4145	0.4514	0.4168
0.4365	0.4189	0.4430	0.4212	0.4496	0.4236	0.4562	0.4260
G12		**G22**		**G32**		**G42**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4261	0.4077	0.4324	0.4100	0.4387	0.4122	0.4451	0.4145
0.4223	0.3990	0.4284	0.4011	0.4345	0.4033	0.4406	0.4055
0.4284	0.4011	0.4345	0.4033	0.4406	0.4055	0.4468	0.4077
0.4324	0.4100	0.4387	0.4122	0.4451	0.4145	0.4515	0.4168
G13		**G23**		**G33**		**G43**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4223	0.3990	0.4284	0.4011	0.4345	0.4033	0.4406	0.4055
0.4185	0.3902	0.4243	0.3922	0.4302	0.3943	0.4361	0.3964
0.4243	0.3922	0.4302	0.3943	0.4361	0.3964	0.4420	0.3985
0.4284	0.4011	0.4345	0.4033	0.4406	0.4055	0.4468	0.4077
G14		**G24**		**G34**		**G44**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4243	0.3922	0.4302	0.3943	0.4302	0.3943	0.4361	0.3964
0.4203	0.3834	0.4259	0.3853	0.4259	0.3853	0.4316	0.3873
0.4147	0.3814	0.4203	0.3834	0.4316	0.3873	0.4373	0.3893
0.4185	0.3902	0.4243	0.3922	0.4361	0.3964	0.4420	0.3985

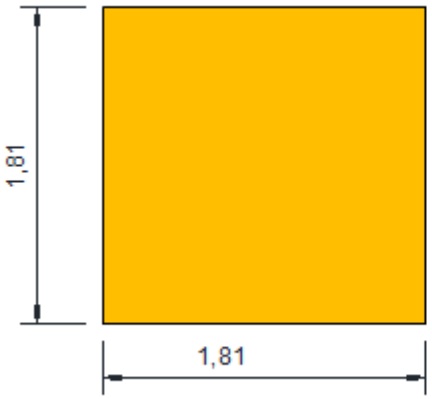
Color Bin Structure

CIE Chromaticity Diagram (Warm White), T_j=85℃, I_F=700mA

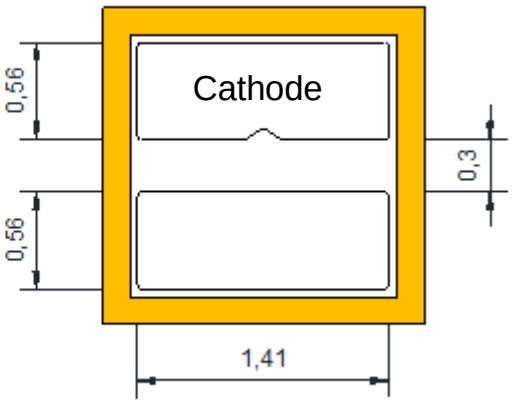


H11		H21		H31		H41	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4562	0.4260	0.4625	0.4275	0.4687	0.4289	0.4750	0.4304
0.4515	0.4168	0.4575	0.4182	0.4636	0.4197	0.4697	0.4211
0.4575	0.4182	0.4636	0.4197	0.4697	0.4211	0.4758	0.4225
0.4625	0.4275	0.4687	0.4289	0.4750	0.4304	0.4810	0.4319
H12		**H22**		**H32**		**H42**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4515	0.4168	0.4575	0.4182	0.4636	0.4197	0.4697	0.4211
0.4468	0.4077	0.4526	0.4090	0.4585	0.4104	0.4644	0.4118
0.4526	0.4090	0.4585	0.4104	0.4644	0.4118	0.4703	0.4132
0.4575	0.4182	0.4636	0.4197	0.4697	0.4211	0.4758	0.4225
H13		**H23**		**H33**		**H43**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4468	0.4077	0.4526	0.4090	0.4585	0.4104	0.4644	0.4118
0.4420	0.3985	0.4477	0.3998	0.4534	0.4012	0.4591	0.4025
0.4477	0.3998	0.4534	0.4012	0.4591	0.4025	0.4648	0.4038
0.4526	0.4090	0.4585	0.4104	0.4644	0.4118	0.4703	0.4132
H14		**H24**		**H34**		**H44**	
CIE x	CIE y	CIE x	CIE y	CIE x	CIE y	CIE x	CIE y
0.4420	0.3985	0.4477	0.3998	0.4534	0.4012	0.4591	0.4025
0.4373	0.3893	0.4428	0.3906	0.4483	0.3919	0.4538	0.3932
0.4428	0.3906	0.4483	0.3919	0.4538	0.3932	0.4593	0.3944
0.4477	0.3998	0.4534	0.4012	0.4591	0.4025	0.4648	0.4038

Mechanical Dimensions

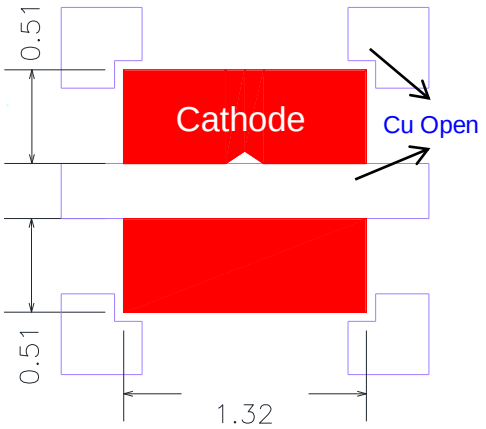


< Top >

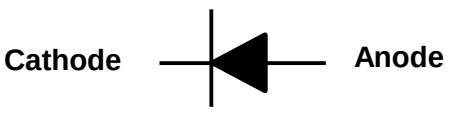


< Bottom >

< Side >



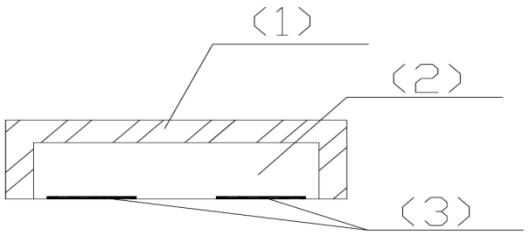
< Recommended Solder Pattern >



< Inner circuit >

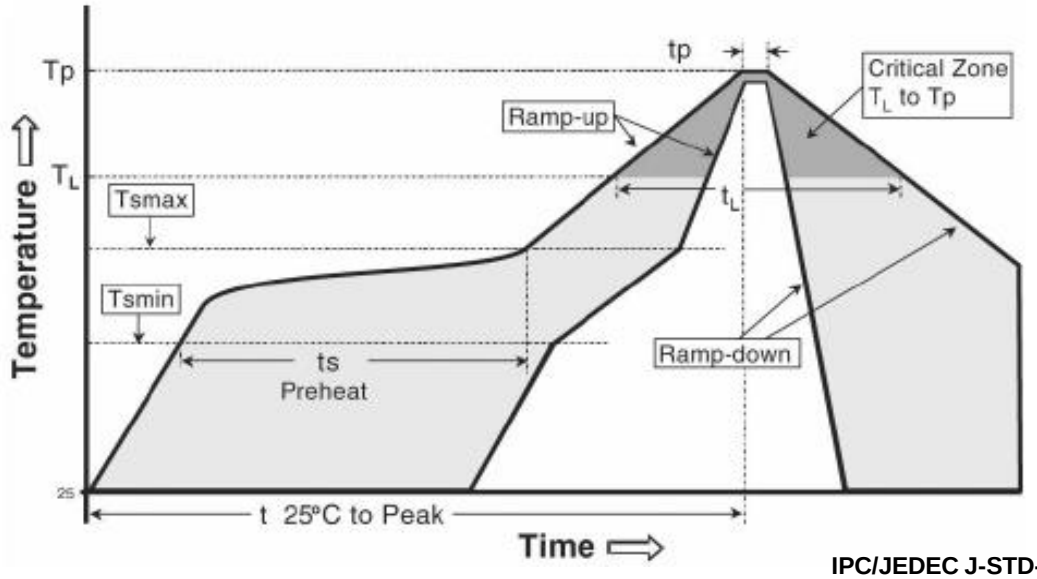
(1) All dimensions are in millimeters.
(2) Scale : none
(3) Undefined tolerance is ±0.2mm

Material Structure



No.	List	Material
①	Encapsulation	Silicone, Phosphor
②	Chip Source	GaN ON SAPPHIRE
③	Solder-PAD	Metal (Au)

Reflow Soldering Characteristics



IPC/JEDEC J-STD-020

Profile Feature	Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)	3° C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (Tsmin to Tsmax) (ts)	 150 °C 180 °C 80-120 seconds
Time maintained above: - Temperature (TL) - Time (tL)	 217~220°C 80-100 seconds
Peak Temperature (Tp)	250~255℃
Time within 5°C of actual Peak Temperature (tp)2	20-40 seconds
Ramp-down Rate	6 °C/second max.
Time 25°C to Peak Temperature	8 minutes max.
Atmosphere	Nitrogen (O2<1000ppm)

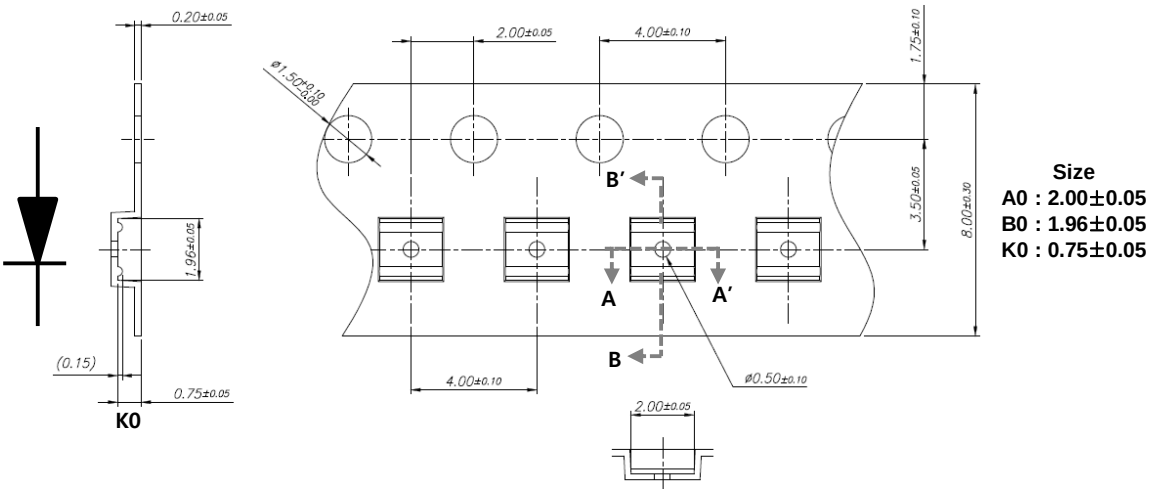
Caution

(1) Reflow soldering is recommended not to be done more than two times. In the case of more than 24 hours passed soldering after first, LEDs will be damaged.
(2) Re-soldering should not be done after the LEDs have been soldered. If re-soldering is unavoidable, LED`s characteristics should be carefully checked before and after such repair..
(3) Do not put stress on the LEDs during heating.
(4) After reflow, do not clean PCB by water or solvent.

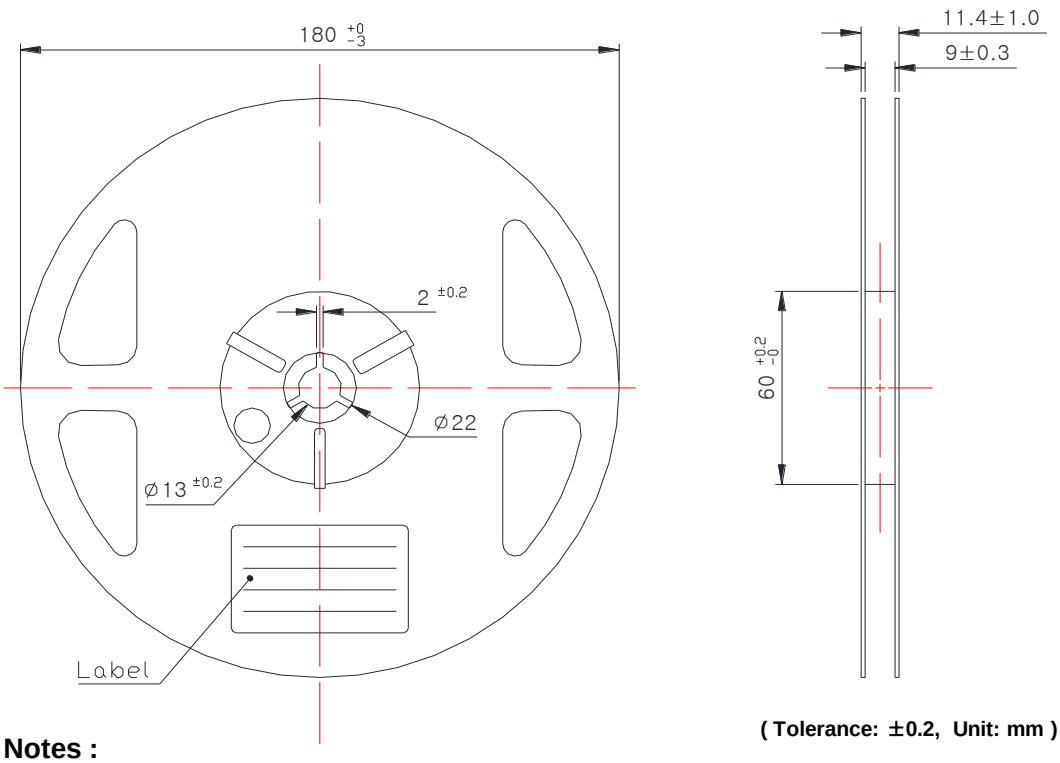
SMT recommendation

(1) After reflow, Over 80% reflectance of PSR is recommended. → Tamura RPW-8000-xx
(2) Solder paste materials (SAC 305, No Cleaning Paste) → Senju M705-GRN360-KV
(3) We recommend TOV Test 1.8v~2.8v at 1uA (per LED)
(4) We recommend IR Test 0~1uA at -5V (per LED)

Emitter Tape & Reel Packaging



Size
A0 : 2.00±0.05
B0 : 1.96±0.05
K0 : 0.75±0.05

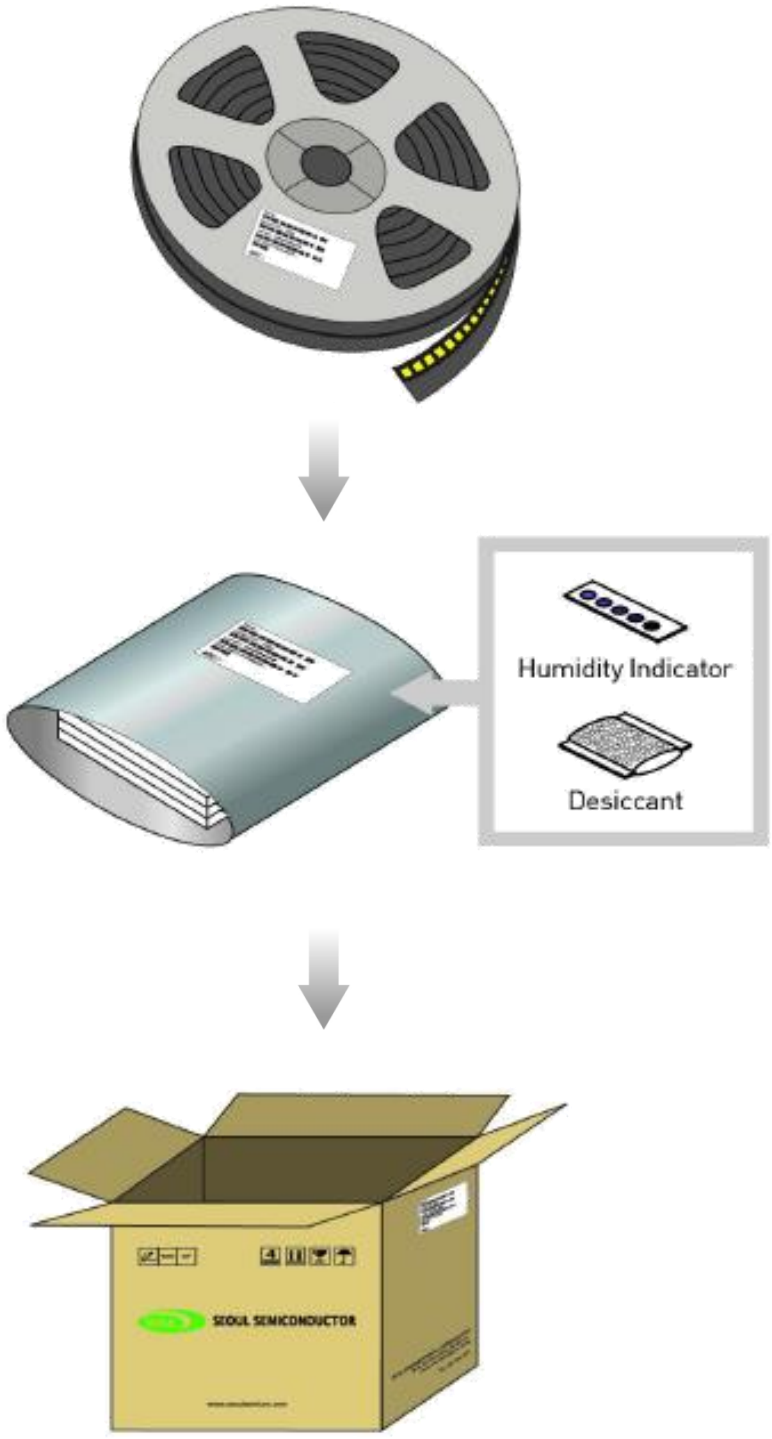


(Tolerance: ±0.2, Unit: mm)

Notes :

(1) Quantity : 1,500pcs/Reel
(empty slot possible in taping reel)
(2) Cumulative Tolerance : Cumulative Tolerance/10 pitches to be ±0.2mm
(3) Adhesion Strength of Cover Tape : Adhesion strength to be 0.1-0.7N when the cover tape is turned off from the carrier tape at the angle of 10º to the carrier tape
(4) Package : P/N, Manufacturing data Code No. and quantity to be indicated on a damp proof Package

Packaging Information



Handling of Silicone Resin for LEDs

(1) During processing, mechanical stress on the surface should be minimized as much as possible. Sharp objects of all types should not be used to pierce the sealing compound.

(2) Do not use tweezers to pick up or handle WICOP LEDs.
A vacuum pick up should only be used.

(3) When populating boards in SMT production, there are basically no restrictions regarding the form of the pick and place nozzle, except that mechanical pressure on the surface of the resin must be prevented. This is assured by choosing a pick and place nozzle which is smaller than the LED's area.

(4) Silicone differs from materials conventionally used for the manufacturing of LEDs. These conditions must be considered during the handling of such devices. Compared to standard encapsulants, silicone is generally softer, and the surface is more likely to attract dust. As mentioned previously, the increased sensitivity to dust requires special care during processing.

(5) Please do not mold this product into another resin (epoxy, urethane, etc) and do not handle this product with acid or sulfur material in sealed space.

(6) Avoid leaving fingerprints on silicone resin parts.

Precaution for Use

(1) Storage

To avoid the moisture penetration, we recommend storing LEDs in a dry box with a desiccant . The recommended storage temperature range is 5℃ to 30℃ and a maximum humidity of RH50%.

(2) Use Precaution after Opening the Packaging

Use SMT techniques properly when you solder the LED as separation of the lens may affect the light output efficiency..

Pay attention to the following:

a. Recommend conditions after opening the package

- Sealing / Temperature : 5 ~ 40℃Humidity : less than RH30%

b. If the package has been opened more than 1 year (MSL 2) or the color of the desiccant changes, components should be dried for 10-24hr at 60±5℃

(3) Do not apply mechanical force or excess vibration during the cooling process to normal temperature after soldering.

(4) Do not rapidly cool device after soldering.

(5) Components should not be mounted on warped (non coplanar) portion of PCB.

(6) Radioactive exposure is not considered for the products listed here in.

(7) Gallium arsenide is used in some of the products listed in this publication. These products are dangerous if they are burned or shredded in the process of disposal. It is also dangerous to drink the liquid or inhale the gas generated by such products when chemically disposed of.

(8) This device should not be used in any type of fluid such as water, oil, organic solvent and etc.

(9) When the LEDs are in operation the maximum current should be decided after measuring the package temperature.

(10) The appearance and specifications of the product may be modified for improvement without notice.

(11) Long time exposure of sunlight or occasional UV exposure will cause lens discoloration.

Precaution for Use

(12) VOCs (Volatile organic compounds) emitted from materials used in the construction of fixtures ca n penetrate silicone encapsulants of LEDs and discolor when exposed to heat and photonic energy. T he result can be a significant loss of light output from the fixture. Knowledge of the properties of the m aterials selected to be used in the construction of fixtures can help prevent these issues.

(13) The slug is electrically isolated.

(14) Attaching LEDs, do not use adhesives that outgas organic vapor.

(15) The driving circuit must be designed to allow forward voltage only when it is ON or OFF. If the rev erse voltage is applied to LED, migration can be generated resulting in LED damage.

(16) LEDs are sensitive to Electro-Static Discharge (ESD) and Electrical Over Stress (EOS). Below is a list of suggestions that Seoul Semiconductor purposes to minimize these effects.

a. ESD (Electro Static Discharge)

Electrostatic discharge (ESD) is the defined as the release of static electricity when two objects come into contact. While most ESD events are considered harmless, it can be an expensive problem in many industrial environments during production and storage. The damage from ESD to an LEDs may cause the product to demonstrate unusual characteristics such as:

- Increase in reverse leakage current lowered turn-on voltage
- Abnormal emissions from the LED at low current

The following recommendations are suggested to help minimize the potential for an ESD event.
One or more recommended work area suggestions:

- Ionizing fan setup
- ESD table/shelf mat made of conductive materials
- ESD safe storage containers

One or more personnel suggestion options:
- Antistatic wrist-strap
- Antistatic material shoes
- Antistatic clothes

Environmental controls:
- Humidity control (ESD gets worse in a dry environment)

Precaution for Use

b. EOS (Electrical Over Stress)

Electrical Over-Stress (EOS) is defined as damage that may occur when an electronic device is subjected to a current or voltage that is beyond the maximum specification limits of the device. The effects from an EOS event can be noticed through product performance like:

- Changes to the performance of the LED package
  (If the damage is around the bond pad area and since the package is completely encapsulated the package may turn on but flicker show severe performance degradation.)
- Changes to the light output of the luminaire from component failure
- Components on the board not operating at determined drive power

Failure of performance from entire fixture due to changes in circuit voltage and current across total circuit causing trickle down failures. It is impossible to predict the failure mode of every LED exposed to electrical overstress as the failure modes have been investigated to vary, but there are some common signs that will indicate an EOS event has occurred:

- Damaged may be noticed to the bond wires (appearing similar to a blown fuse)
- Damage to the bond pads located on the emission surface of the LED package
  (shadowing can be noticed around the bond pads while viewing through a microscope)
- Anomalies noticed in the encapsulation and phosphor around the bond wires.
- This damage usually appears due to the thermal stress produced during the EOS event.

c. To help minimize the damage from an EOS event Seoul Semiconductor recommends utilizing:

- A surge protection circuit
- An appropriately rated over voltage protection device
- A current limiting device